On the Design of Wideband CDMA User Equipment (UE) Modem

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Abstract— **This paper describes the details of the implementation issues on wideband CDMA UE Modem, concentrating on the receiving side. Employed top-down design methodology and corresponding work efforts on each task are stated to demonstrate the effectiveness of the methodology.**

Keywords— **WCDMA, 3GPP, UE Modem.**

I. Introduction

Design methodology and the technical details of 3GPP Compliant UE Modem, which has been implemented based on [1]-[6], are treated in this paper. Basically, this Modem has been tested including following advanced features on down-link (DL):

- Tx Diversity
  - Open-Loop (OL) Diversity : Space Time Transmit Diversity (STTD) & Time Switched Transmit Diversity (TSTD)
  - Closed-Loop (CL) Diversity : Mode 1 & 2
- Power Control
  - Down-Link Power Control (DL PC)
  - Up-Link Power Control (UL PC)
  - Site Selection Diversity Transmit Power Control (SSDT)
- Compressed Mode (CM)
- including AICH / PICH / CPCH-related Indicate Channels (ICHs) / PDSCH
- upto 3 MultiCodes (MCs)

On up-link (UL) side, DPCH supports upto 6 MCs.

II. Design Methodology

From the specifications to the test of the implemented system, tasks are categorized as follows.

- Task 1 : Specifications & Requirement Analysis
- Task 2 : Floating-Point Modeling
- Task 3 : Fixed-Point Design
- Task 4 : VHDL & SW Implementation
- Task 5 : Prototyping & Test

Task 1, Specifications & Requirement Analysis, denotes the overall system specifications in terms of functionality which might be implemented and the requirement analysis of the target hardware, e.g., FPGA & ASIC, u-Controller, analog front-end (AFE) etc. Verification and test plan of successive tasks can also be developed during this task.

Task 2, Floating-Point Modeling, means the reference functional model development. This task should be achieved by considering the performance and complexity simultaneously to select the potential algorithm. High-level design tool could be adopted to ease the overall design and verification process.

Task 3, Fixed-Point Design, is the development of the architectural model development. Output of this task, i.e., fixed-point design, is compared with the floating-point model in terms of performance with determined bit-width of design. HW & SW partitioning should be done within this task. Exactness of fixed-point design and VHDL implementation can be managed due to the work efforts of design & test stage. Same design environment as in Task 2 might reduce the design efforts of Task 3.

Task 4, VHDL & SW Implementation, is the task of implementation regarding HW & SW. Design environment in terms of top-down solution might help the overall approach. Various Co-Simulation strategy for the fixed-point model & VHDL model and/or the HW & SW could be set up. In case of SW implementation, requirements of SW task and interfaces with HW should be carefully treated.

Task 5, Prototyping & Test, includes prototype system design, such as FPGA/ASIC-based system, and functional & performance test of the prototype system. Development of the appropriate test environments is also the part of this task. This test phase can be divided into stand-alone and system-level integrated test.

Feedback to the previous steps should always be allowed.

Work efforts among the tasks on the design of the wideband CDMA UE modem are roughly as follows. Task1 : Task2 : Task3 : Task4 : Task5 = 2 : 1 : 3 : 3 : 6.

III. UE Demodulator

We focus our discussion on the downlink receiving side first, i.e., UE demodulator. Top-level architecture of UE demodulator is shown in Fig. 1.

A. Digital Front-End (DFE)

DFE consists of matched filter (MF), down-sampling to appropriate rate by decimation, up-sampling to 8/Tc by interpolation, DC offset compensation and DAGC. The ADC output signal, which is provided at 8/Tc, is down-sampled to 4/Tc, then filtered by the digital matched filter. This front-end decimation filter let the matched filter consume less power. The matched filter output rate is reduced by a factor of 4 to 1/Tc by a sampling device and provided

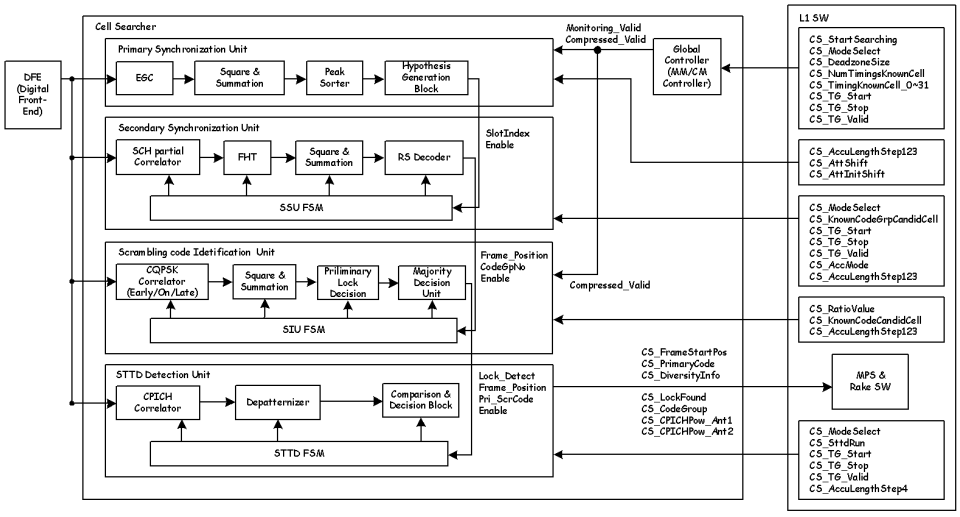

Fig. 3. Top-level architecture of CS.

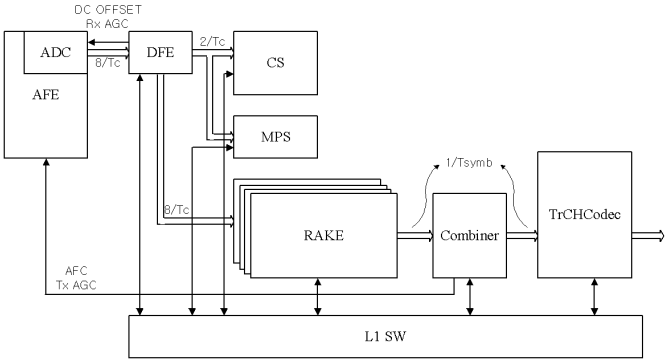

Fig. 1. Top-level architecture of UE demodulator.

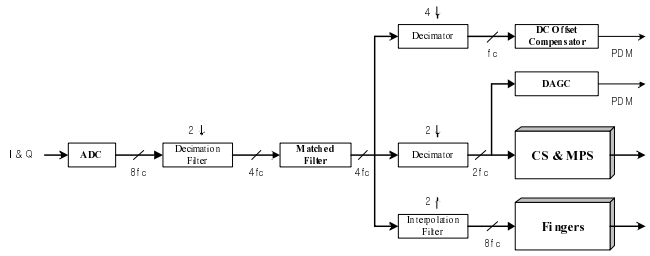

Fig. 2. Top-level architecture of DFE.

as an input of DC offset compensator. A DC offset on the matched filter output is removed by the DC offset control loop. The DC offset at the matched filter output (resulting from analog DC voltages, AD-conversion and truncation in the matched filter) is computed by the offset compensation block. To control the receiving power of UE, the power at the matched filter output, after decimating by a factor of 2 to 2/Tc, is monitored by the DAGC. The DAGC generates a sigma-delta modulated control signal for an external gain controlled amplifier to keep the matched filter (and frontend) output power at a constant average level. The control signal for the analog offset compensation circuits is provided via sigma-delta modulation to close the mixed analog/digital offset compensation loop. The DAGC error level and the power level is provided as outputs, to be read by the u-Processor to derive input power measurements. This 2-times decimated matched filter output also becomes the input of cell searcher (CS) and multipath searcher (MPS).

An interpolation filter increases the sampling rate at the matched filter output from 4/Tc to 8/Tc, by means of digital interpolation to provide data at higher sampling rate to Rake finger.

The top-level architecture of DFE is given in Fig. 2.

B. Cell Searcher (CS)

In general, the CS, which results from the asynchronous behavior of the 3GPP network, searches over monitored and unlisted cells. Initial cell search, which is the task the UE has to perform first after power-on, is specifically related to the search of camping cell. In addition to the initial acquisition, the CS performs monitoring mode operation to monitor neighboring cells up to 32 by peak nulling method, which is necessary to identify possible candidates for either soft handover (SHO) or hard handover (HHO). The search for SHO candidate cells is performed on the same carrier frequency, which is currently used by the camping BTS, while the search for HHO candidates is performed on different carrier frequencies upto 8. For that purpose, the camping BTS uses the feature of DL compressed mode (CM) to switch to that new target frequency during several slots of transmission gap.

The acquisition procedure consists of three major steps and an additional step to detect the use of transmit diversity in the BTS. These four steps are

- 1st Step : Slot Timing Identification by PSC
- 2nd Step : Frame Timing & Scrambling Code Group Identification by SSC
- 3rd Step : Scrambling Code Number Identification
- 4th Step : STTD Detection

CS global controller generates control signals out of a set of timing information given by the L1 SW. These control

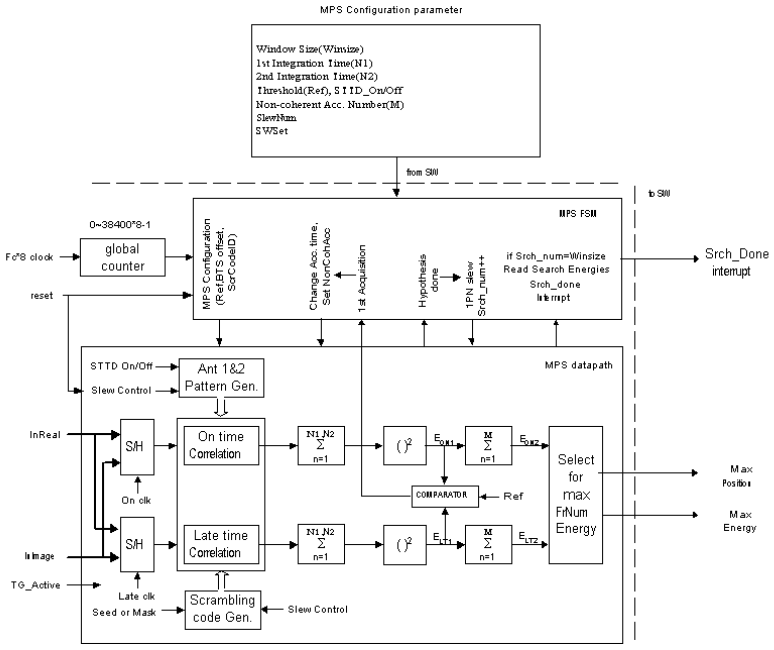

Fig. 4. Top-level architecture of MPS.

signals steer the acquisition procedure for all different operational modes of normal mode (NM), monitoring mode (MM) and compressed mode. The Top-level architecture of CS is given in Fig. 3.

Each step has its own task, relies on intermediate results of the preceding step, and initiates the operation of the next step. All timing information that result from the cell searching operations or that are given to the CS by the SW as a priori knowledge have an accuracy of Tc/2. All absolute timing values are related to a UE global time reference: a counter that is running from 0 to (15 · 8 · 2560 - 1) at 8/Tc. Since the accuracy of this counter is higher than the accuracy of the CS timing, a modified time based signal is fed into the CS.

The PSC unit has the task to process a configurable amount of input data and generate eventually a hypothesis on the timing of the slot boundaries in the received MF output signal, a value between 0 and (2 · 2560 - 1), together with an activation signal for the 2nd step. This PSC unit concerns all the operational modes of NM, MM and CM. Then, SSC unit copies the hypothesis for the slot boundary into an internal register and generates hypotheses on frame boundary timing, a value between 0 and (15 · 2 · 2560 - 1), and on scrambling code group, a value between 0 and 63, together with an activation signal for the 3rd step. Then, the 3rd step copies these values to internal registers and tries to identify the used scrambling code inside the group reported by the 2nd step. If this operation ended successfully, the found absolute scrambling code number, a lock-found indicator, and the used timing information with an activation signal for the 4th step are generated. Then, the 4th step tries to detect whether STTD was used in the BTS transmitter and generates values that can be used to compute the CPICH power. The 4th step covers frequency error upto ± 3 ppm, i.e., ± 6 KHz. Denote CPICH is employed instead of SCH for STTD detection in this paper.

The 2nd ∼ 4th steps only concern the operational modes of NM and MM. The operations and communications described above result in one-way handshaking from the 1st to the 4th step. This control flow mechanism is more efficient than synchronizing the steps to a fixed timing grid that is spaced with the least common multiple timing of all units.

C. MultiPath Searcher (MPS)

The MPS establishes and updates the profile of the channel and selects echoes for further processing, i.e., tracking for demodulation, in the rake receiver based on the channel profile for 6 ∼ 8 active set members. The MPS is composed of several functions that are described follow :

- Correlator Bank
- Non-Coherent Accumulator
- Echo Selection Block

The searcher engine searches strong echo signals in pair, evaluating the energy at both the current searcher position (On-Time) and a half PN chip delayed from the on-time position (Late-Time). Important performance criterion for MPS is searching time and its reliability. For fast searching the correlation length should be reduced as small as possible, and for reliability the correlation length should be increased as much as possible. For fast searching and high reliability simultaneously, we employ two different correlation lengths N_1 and N_2, where N_2 is greater than N_1. The resolution of N_1 and N_2 is Tc for each On-Time & Late-Time. If search energy for the correlation length N_1 is less than the threshold value given by SW, then searcher slews to the next position and starts correlation for this position. If search energy for the correlation length N_1 is

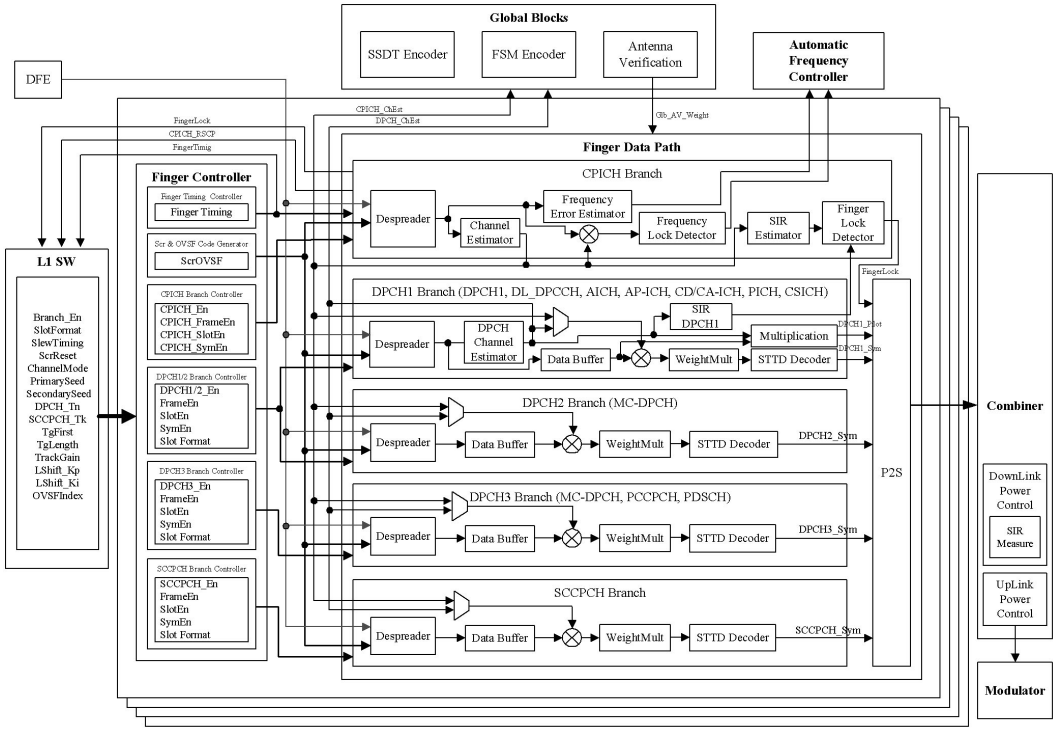

Fig. 5. Top-level architecture of Rake receiver and combiner.

greater than the threshold value, then searcher increases correlation length from N_1 to N_2 for that position. By using longer correlation length, detection probability can be increased and false alarm probability can be reduced. So, the double dwell serial searching algorithm can achieve fast searching time and reliability simultaneously. For more reliability, post-detection integration, i.e. non-coherent accumulation by M, is used additionally. That is, the total searching time per active member cells is the function of searching window size (L), correlation length (N_1, N_2), number of post-detection integration (M), number of multipaths and number of active cells. Fig. 4 shows the top-level architecture of MPS.

The MPS consists of two major elements, the control finite state machine (FSM) and the datapath. The SW configures the FSM by writing window size, N_1, N_2, M, threshold values, slew number and STTD_on, etc. The FSM forces the according generator set, consisting of scrambling code generator, OVSF code generator and pilot pattern generator, to slew to the correct search starting position. For search operation, the FSM looks for the next even CPICH symbol. If this occurs, the search over window size will be started. During this search, the FSM forces the other generator set to slew to the given search starting position. If one search is finished, the next search will be done with the other generator set. This dual generator set enhances the searching time performance, especially during SHO. Also, the FSM writes a SearchDone signal as a L1 SW interrupt. Due to this, the L1 SW read the echo energy values and the according echo positions upto 4.

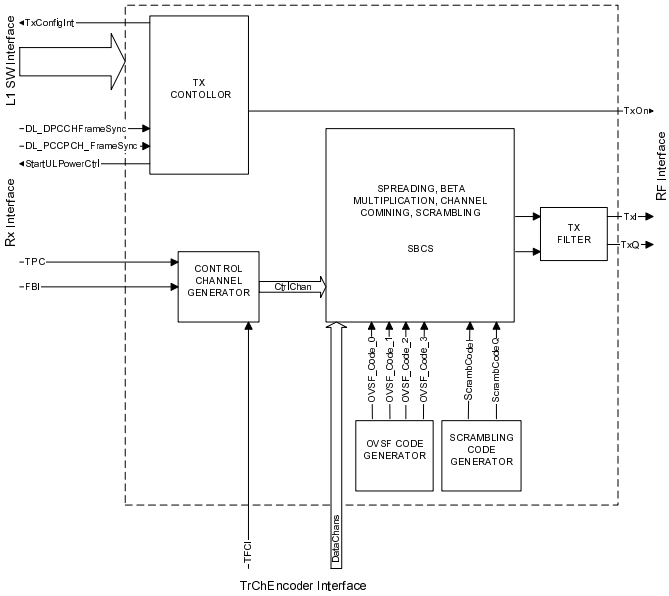

Fig. 6. Top-level architecture of modulator.

D. Rake Receiver and Combiner

Fig. 5 shows the top-level architecture of Rake receiver and combiner. The L1 SW running on the u-Processor is responsible for finger assignment and finger control. The L1 SW gets information on the current finger state from the 4 Rake fingers and information on the available echoes in the transmission channels for all base stations in the active set from the MPS. The set of selected echoes from

the MPS is determined by L1 SW. The information on echo power, base station ID and echo timing are updated by the interaction of L1 HW, L1 SW and high layer configuration.

There are 5 branches in the Rake receiver (per finger) and combiner.

- DPCH1 (DPCH1, DL-DPCCH, AICH, AP-ICH, CD/CA-ICH, PICH, CSICH)
- DPCH2 (DPCH2)
- DPCH3 (DPCH3, PCCPCH, PDSCH)
- SCCPCH (SCCPCH)
- CPICH for Rake or DPCH1Pilot for Combiner (dedicated DPCH1 branch for pilot symbols only)

The fingers perform channel estimation, physical channel demodulation, timing error detection and time tracking, and SIR and received signal code power (RSCP) estimation for finger lock detection. The feedback signalling message (FSM) encoder calculates the FSM information based on the channel estimations obtained from CPICH despreading for all fingers. The frequency error detector calculates estimates for the current frequency offset based on the channel estimations obtained from CPICH despreading for all fingers. The antenna verification unit is active only for closed-loop tx diversity Mode 1. Antenna verification is performed based on the CPICH and DPCH based channel estimates in all active fingers. The antenna verification block feeds back the weights to be applied to the CPICH based channel estimation when applied to the demodulation of DPCH/PDSCH channels. UL and DL power control (PC) for DPCH are also the part of RAKE functionalities.

The combiner block performs coherent combining of the weighted and time-aligned demodulator output symbols, which are one type of user data with control information (e.g. DPCH) or pure control information (AICH, PICH). The combiner combines the received signal and demultiplexes user data and control information, i.e., user data to TrCH and TPC information to power control, etc. The combiner performs 3 tasks in the branches.

- Time Alignment of the Received Data in De-Skewing Buffer
- Combining of the Data in Data Combining Unit
- Decoding of Indicator Channels (AICH, PICH, etc. in DPCH1 Branch only) in Indicator Channel Decoding Unit (in DPCH1 Branch Combining Unit)

For DPCH channels, this function is performed independent of the base station ID (i.e., for all active set members), while for all other channels, the combining is restricted to the set of fingers assigned to the echoes coming from one particular base station. The finger output symbols to the combiner are declared valid if the finger is enabled and the finger slewing procedures are finished, such that only useful symbols are actually taken into account for combining. In addition, the finger output symbols can be declared invalid if the finger is out-of-lock. This can be used to ensure a certain quality of the finger output symbols considered for combining.

IV. UE Modulator

Fig. 6 shows the top-level architecture of the modulator. The modulator supports upto 6 MCs, and it contains on-chip RRC filter. The modulator consists of the following functional blocks.

- Tx Controller
- Control Channel Generator
- OVSF Code Generator
- Scrambling Code Generator
- Spreading, Scrambling, Beta Multiplication, Channel Combining and Spreading
- Tx RRC Filter

The modulator has its interface with Demodulator, TrChEncoder, RF and L1 SW of the modulator.

V. Conclusions

Design of 3GPP Compliant UE Modem, which has been implemented by top-down approach, has been described in this paper. Details of the Modulator and the Demodulator of DFE, CS, MPS, Rake and Combiner are treated. All the functions described in this paper have been tested successfully.

Acknowledgment

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References

[1] 3G TS 25.201 : "Physical Layer - General Description." Release 1999.
[2] 3G TS 25.211 : "Physical Channels and Mapping of Transport Channels onto Physical Channels (FDD)," Release 1999.
[3] 3G TS 25.212 : "Multiplexing and Channel Coding (FDD)," Release 1999.
[4] 3G TS 25.213 : "Spreading and Modulation (FDD)," Release 1999.
[5] 3G TS 25.214 : "Physical Layer Procedures (FDD)," Release 1999.
[6] 3G TS 25.215 : "Physical Layer - Measurements (FDD)," Release 1999.