

# H-Ternary Line Decoder for Digital Data Transmission: Circuit Design and Modelling

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## Abstract

The design method of the H-ternary line decoder is given. A simulation model of the designed decoder is realised using Circuitmaker package. This is supplemented with a prototype model for operational verification purpose. The decoder consists of a design of the clock recovery circuit. The latter is an essential part for synchronising the decoder with the encoder for the purpose of exact sampling instant of the incoming symbols. The results obtained from both simulation and prototype models are found in quite agreement with each other and with the theory.

*Keywords: Line codes, Data transmission, Digital signal processing, Networks, Clock recovery, Simulation, Modelling.*

## I. Introduction

Recently, digital data transmission has witnessed a considerable importance. This is a result of the huge increase in applications where data, voice, video, and multimedia are digitally processed. Digital modulation, baseband or passband or both, is the mean by which information can be transmitted through networks that are either wire-connected or wireless. In contrary to passband, where usually sinusoidal carriers are used, baseband modulation is the process of direct transmission of digital signal without spectrum transformation. In baseband modulation, however, the pulse waveform (mostly in PCM) is modified in such a way as to suite the transmission medium and thus often called line coding. A variety of line code waveforms have been proposed in the literatures.

An effort is made to find codes with some desirable properties such as small bandwidth with no dc content, adequate timing information, power efficiency, transparency, and with error detection and correction capability. A general form of line code is a multilevel waveform. Binary, ternary and quaternary line codes are special cases when two, three, and four levels are used respectively for signal representation. Preliminary studies of some of the line codes are treated in [1-4], where comparison is made based on their desirable features. Most recent survey of line codes that are used in modern telecommunication networks such as ISDN, ATM, FR and the newly emerged xDSL can be found in [5-7].

The new hybrid (H)-ternary line coding scheme is derived from three well-known line codes: NRZ-L, dicode, and polar RZ. H-ternary line code operates on a hybrid principle between these three codes. A detailed encoding scheme of the H-ternary line code can be found in [7,8], however, the operation summary will be given in next section. The design method and simulation of the encoder is also treated fully in [8].

In this paper, the design of H-ternary line decoder together with its clock recovery circuit is given. Next section provides a description of the encoding and decoding schemes of the new line code. Section three gives details of the design method using digital and analogue technologies. Simulation and prototype models of the designed decoder circuits are given in section four. Section five provides the design method of the clock recovery circuit. Finally, the discussion and conclusion are given in section six.

## II. Encoding and Decoding Principles

### II.1. Encoder Operation

The H-ternary line code operates on a hybrid principle that combines the binary NRZ-L, the ternary dicode and the polar RZ codes and thus it is called hybrid-ternary. The states table shown in figure (1) depicts the encoding procedure. The H-ternary code has three levels for signal representation; these are positive (+), zero (0), and negative (-). These three levels are represented by three states. The state of the line code could be in any one of these three states. A transition takes place to the next state as a result of a binary input 1 or 0 and the encoder output present state. The encoding procedure is as follows:

- (1) The encoder produces + level when the input is a binary 1 and whether the encoder output present state is at 0 or – level.
- (2) The encoder produces – level when the input is a binary 0 and whether the encoder output present state is at 0 or + level.
- (3) The encoder produces 0 level when the input is binary 1 and the encoder present state is + level or when the input is binary 0 and the encoder present state is – level.
- (4) Initially, the encoder output present state is assumed at 0 level when the first bit arrives at the encoder input.

Above procedure gives the reader a sufficient information about the operation of this new line coding scheme. Further details and comparison together with design and modelling of the encoder can be sought from references [7,8]. The variation of this new line code is that it violates the encoding rule of NRZ-L and dicode when a sequence of 1s or 0s arrives. In the latter case, it operates on the same encoding rule of polar RZ but with pulse occupancy of full period.

Input Binary	Output Ternary	
	<i>Present State</i>	<i>Next State</i>
1	0	+
1	-	+
1	+	0
0	-	0
0	0	-
0	+	-

Figure (1) Encoder output states table.

### II.2 Decoder Operation

Figure (2) shows the states table of the H-ternary decoding procedure. It is a reverse process of the encoding operation given in the previous

subsection. The decoder has only two output states (binary) whereas the input is three states ternary. The decoding procedure is as follows.

- (1) The decoder produces an output binary 1 when the input ternary is at + level and whether the decoder output present state is a binary 1 or 0.
- (2) The decoder also produces an output binary 1 when the input ternary is at 0 level and the decoder output present state is at a binary 1.
- (3) Similarly, the decoder produces an output binary 0 when the input ternary is at – level and whether the decoder output present state is a binary 0 or 1.
- (4) Finally, the decoder produces an output binary 0 when the input ternary is at 0 level and the decoder output present state is a binary 0.

It is clear that the decoding process at the receiver is quite similar to that of the NRZ-L code when the + and - levels are received. The difference arises when level 0 is received. In which case, the decision is made depending on the decoder output present state.

Input Ternary	Output Binary	
	<i>Present State</i>	<i>Next State</i>
+	1	1
+	0	1
0	1	1
0	0	0
-	0	0
-	1	0

Figure (2) Decoder output states table.

## III. Decoder Circuit Design

The decoder circuit is designed using the truth table shown in Figure (3). The states table is a modified version to that table shown in figure (2) where the input ternary states are represented by a 2-bit binary A and B. The binary states 01, 00, and 10 are assigned to the +, 0, and – input ternary states/levels respectively. In previous representation, the binary state 11 will not occur and thus is taken as don't care state. The decoder input is a ternary waveform whereas its output is the binary pseudo-random (PN) sequence waveform that is generated and then encoded at the transmitter. The input ternary in 2-bit binary form representation is used in order to simplify the implementation of the decoder circuit using a digital technique. The digital part involves the design of a combinational logic circuit using the truth table shown in figure (3).

The next state  $C_n$  using K-map or Boolean algebra minimisation is given by

$$C_n = \overline{B}(A + C_p),$$

where the variables  $A$  and  $B$  represent the 2-bit input ternary and  $C_p$  and  $C_n$  are the binary output present and next states respectively.

A memory element is used in a form of D-type flip-flop to provide the feedback required for the operation of the decoder and also to obtain the recovered/decoded binary sequence output. Figure (4) shows the designed decoder which consists, in addition to the digital part, a reconditioning analogue and clock recovery parts.

The digital designed part in figure (4) is preceded by an analogue part. The function of the analogue part is to split and reconditions the incoming H-ternary signal into two-binary format waveforms  $A$  and  $B$  at the decoder input. The splitting circuit consists of a 2-diode with opposite polarity connection to a common end. This circuit produces the binary variables  $A$ , and (negative shifted)  $B$  at the other ends. A reconditioning unity gain inverting amplifier, which also acts as interfacing circuit, is used to invert the phase of variable  $B$  to become in TTL format. Another buffer circuit is also used to interface the analogue part to the digital part at input binary  $A$ . The decoder complete circuit is shown in figure (5).

Input Ternary		Output Binary	
		<i>Present</i>	<i>Next</i>
$A$	$B$	$C_p$	$C_n$
1	0	1	1
1	0	0	1
0	0	1	1
0	0	0	0
0	1	0	0
0	1	1	0

Figure (3) Decoder binary truth table.

#### IV. Design Modelling

A simulation model for the circuit that is designed in the previous section has been implemented to investigate its operation. Circuitmaker simulation package [9] has been used to achieve this objective prior to its hardware implementation. Figure (5) shows the simulation-working place of the decoder together with the additional analogue circuits.

The circuit is driven by stimuli which is an H-ternary signal taken from the encoder [8]. Probes at different points on the simulation model are used to provide the input/output waveform at each stage. Figure (6) depicts the H-ternary encoded waveform applied at the decoder input together with the regenerated clock and recovered binary PN sequence waveforms. It is evident that these waveforms are in exact agreement with the decoding principles. The recovered PN sequence has one bit delay compared to the input H-ternary

line code. This delay arises from the fact that the decoder circuit has a memory element, which makes correlation between the present binary output and the present ternary input to make decision for the next binary output. The recovered PN sequence has 2-bit delay in comparison with the original input sequence at the encoder input. The 2-bit delay is a result of the two memory elements used at both the encoder and decoder circuits.

The simulation model is also supplemented by a prototype decoder circuit in order to validate its operation. The waveforms obtained from the hardware model are in exact agreement with that of the simulation model.

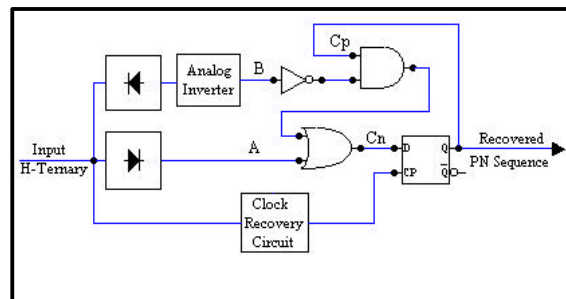


Figure (4) Designed decoder circuit.

#### V. Clock Recovery Circuit Design and Modelling

The decoder circuit needs clock signal for proper operation. The clock signal should be recovered or regenerated at the receiving end from the incoming signal. One of the prime desirable features of H-ternary line code is its richness in timing information. This makes the clock regeneration method simple. Figure (7) shows the simulation-working place of the complete designed clock recovery circuit. It consists of a differentiator, full-wave rectifier, an adder, and a monostable multivibrator together with other buffering/interfacing circuits. The clock recovery circuit from the incoming H-ternary line code is operationally realised using simulation technique shown in figure (7). It is also then implemented in hardware to verify its operation. The circuit output, which is the required clock, is shown in figure (6) together with the recovered PN binary sequence. This clock is used to provide triggering signal to the flip-flop of the decoder at the proper time instants.

#### VI. Discussion and Conclusion

The H-ternary line code has been derived from NRZ-L, dicode, and polar RZ codes to counter some of their deficiencies. NRZ-L and dicode codes lack sufficient timing information when the input signal remains at one binary level. This has

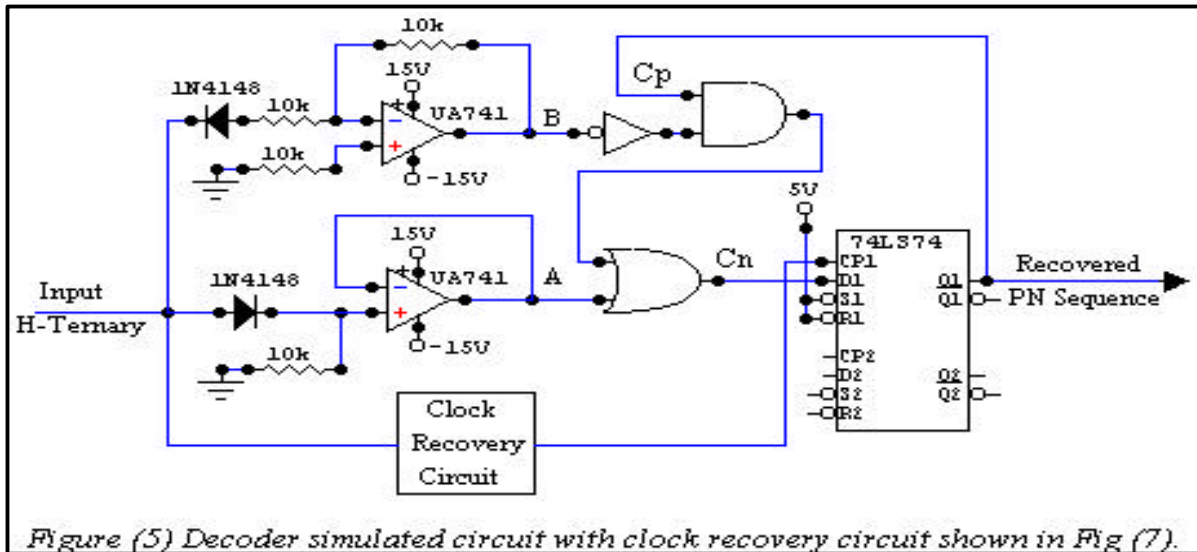


Figure (5) Decoder simulated circuit with clock recovery circuit shown in Fig (7).

direct influence on clock recovery and then on synchronising the receiver with the transmitter. It is also directly affecting the detection of the received digital signal.

The H-ternary line code has power spectral density superiority in comparison with the polar RZ code. The latter has its frequency spectral components concentrated at the original binary data rate. This is due to the fact that the polar RZ code has a pulse duty cycle of 50 percent. However, the power spectral density of the new line code is concentrated at half the original binary data rate. It is also having low level spectra closer to the zero frequency (dc) compared to both polar RZ and NRZ-L line codes.

The H-ternary line code is a type of correlative codes. Such a code has the ability to detect single error at receiver, however, it is also duplicate error whenever it occurs. This correlative property however, duplicates error if it happens as well. The latter is considered as one the drawback of such line code when the binary data at encoder input is not using channel error control coding schemes to protect transmitted signal against noise and other impairments on the transmission channel. The performance operation of the decoder with regarding to immunity against noise and hence the probability of error needs further theoretical investigation.

The hardware of the encoder and decoder circuits is integrated to form a transceiver. This enables a user to encode and decode binary data and ternary received signal respectively. Further work for the modification of the integrated transceiver is needed toward the implementation of an ASIC form for commercial application.

In conclusion, the decoding procedure of the H-ternary line code scheme is presented together with its encoding procedure. The decoder circuit together with its clock recovery circuit are designed

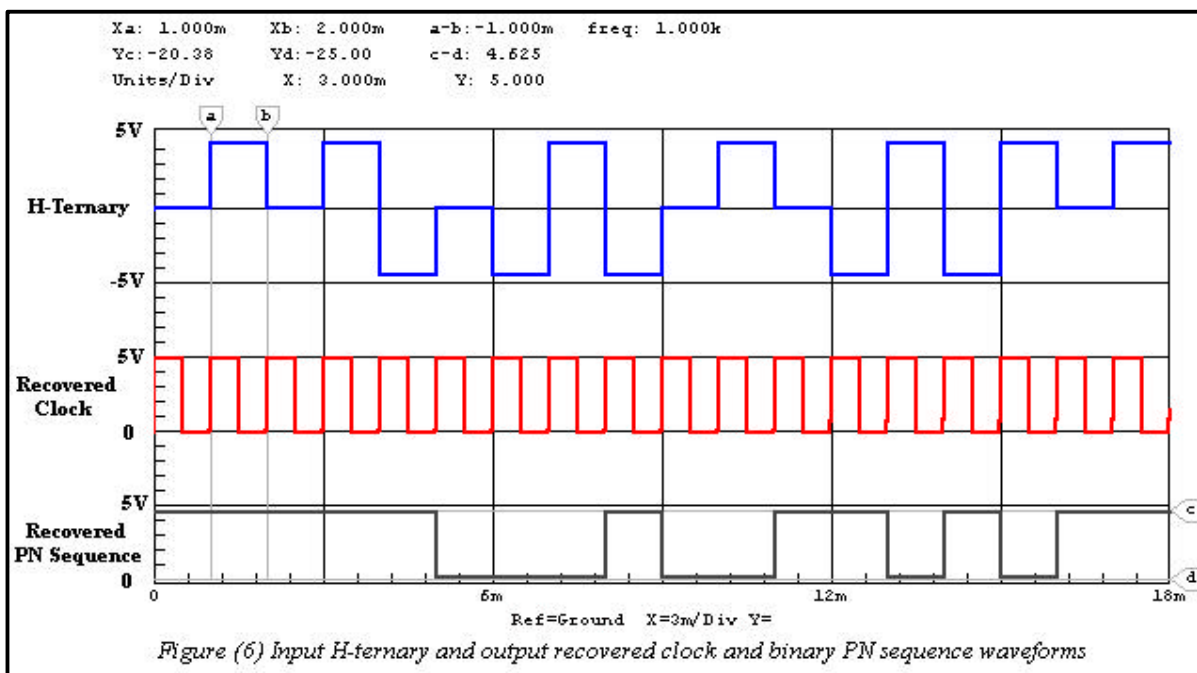


Figure (6) Input H-ternary and output recovered clock and binary PN sequence waveforms

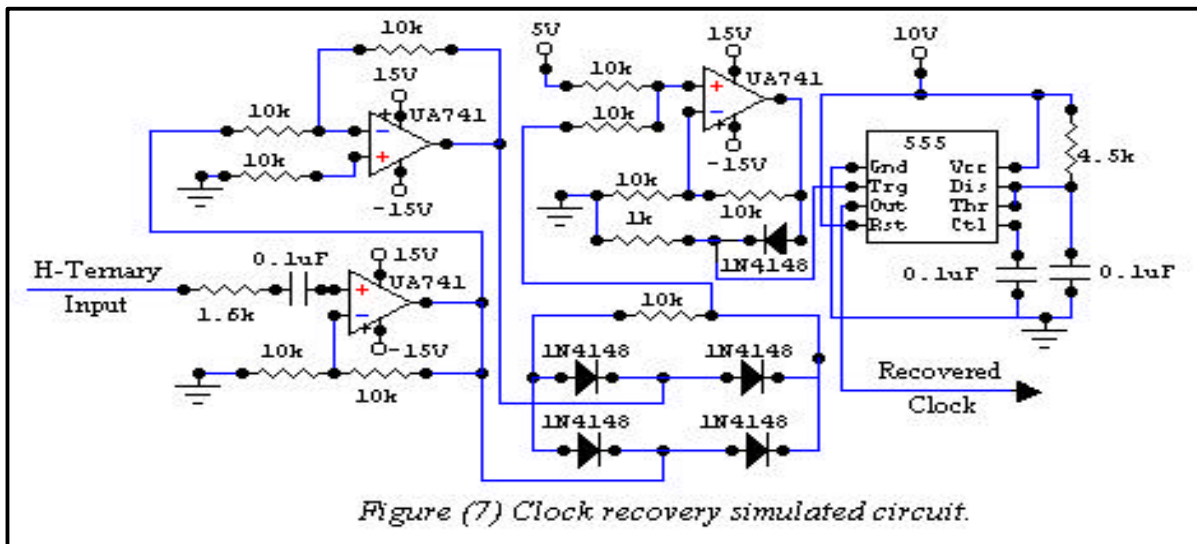


Figure (7) Clock recovery simulated circuit.

and then operationally tested. The test-bed is achieved using simulation and prototype techniques. The results obtained from both models satisfy each other and with the theoretical one. Finally, its pros and cons in comparison with its counterparts are discussed.

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