Modular Software Receiver for Radio Signal Analysis

Jerzy Lopatka Ph.D.
Communications Systems Institute
Military University of Technology, Warsaw, Poland
e-mail: jlopatka@wel.wat.waw.pl

1. Abstract

This paper presents a scalable modular software receiver (MSR) for technical analysis of radio emissions. It enables acquisition, recording, recognition and demodulation of various types of radio signals. It is based on Texas Instruments TMS 320c67 digital signal processors.

2. Introduction

Software radio is a concept of a dedicated computer system, that can be programmed to perform functions corresponding to current user needs in a wireless communications area [1][2]. Such a type of radio can be used as a general purpose equipment to achieve interoperability with a range of communications systems, local area networks, warning networks etc. They can be also used for radio monitoring systems, surveillance systems and electronic warfare purposes.

The proposed receiver is based on digital signal processing circuits. Its hardware consists of dedicated PCI or CPCI boards. They are used for analog signal conditioning, converting into digital form, filtration and decimation. Main tasks, related to signal analysis, recognition and demodulation, are performed by DSP-s. Frequency range, bandwidth of analysis, mode of operation and processing power of the radio can be adjusted by selecting an appropriate number of specified boards.

Radio analysis software is also a modular application. Its functions and performance depend on installed hardware and current application.

3. Hardware configuration

The MSR consists of five functional blocks (fig. 1) :
- an analog signal conditioning block and ADC, working with 65 MHz sampling frequency;
- narrowband digital tuners with bandwidth up to 2 MHz;
- wideband digital tuners with bandwidth up to 25 MHz;
- a delay line with up to 512 MB RAM capacity, providing delay up to 2 seconds;

- DSP boards equipped with up to 4 DSP-s each.
All these blocks are implemented in three types of boards: analog signal conditioning, ADC and narrowband tuner board (NTB), delay line and wideband tuner board (WTB), and DSP board. All these boards can work synchronously and they are interconnected by four types of buses:
- ADC BUS - 12/24 bits wide parallel bus, with clock frequency 65 MHz. The lower part of the bus is used for transmission of the output signal directly from ADC. The signal can be used e.g. by several tuners of the multi-channel receiver. The upper part of the bus can be used for transmission of the delayed ADC signal. It is very useful for searching receivers, monitoring solutions etc.
- Coreco's Auxiliary BUS (CAB) – 32-bit bus working at 50 MHz. It is a basic bus for communications between tuners and DSP boards and between different DSP boards.
- Serial buses that are the 50 MHz dedicated links between specified DSP-s and other boards. They can be used for receiver tuning, AGC control etc.
- PCI or CPCI bus that is mainly used for boards programming purposes, but it can also be used either for the tuners output signals storage on the HDD or playback of previously recorded signals. CPCI version is dedicated for ruggedized solutions.

MSR hardware can be configured according to the current needs. In the simplest case, if we want to process only simple, fixed frequency narrowband signals, the MSR contains only the NTB board. An input analog signal is converted into digital form, mixed with local oscillator, decimated and filtrated. The output signal is passed through the PCI interface into the PC memory and is processed by the PC processor. For more complex cases, additional computational power is provided by the DSP board. Down-converted signal is transmitted to the DSP using CAB. DSP can also control amplifiers, filters and a tuner using dedicated serial bus.

The WTB board can be used for reception of wideband signals. Because of the high data rate, on its output, it works with one or more DSP boards.
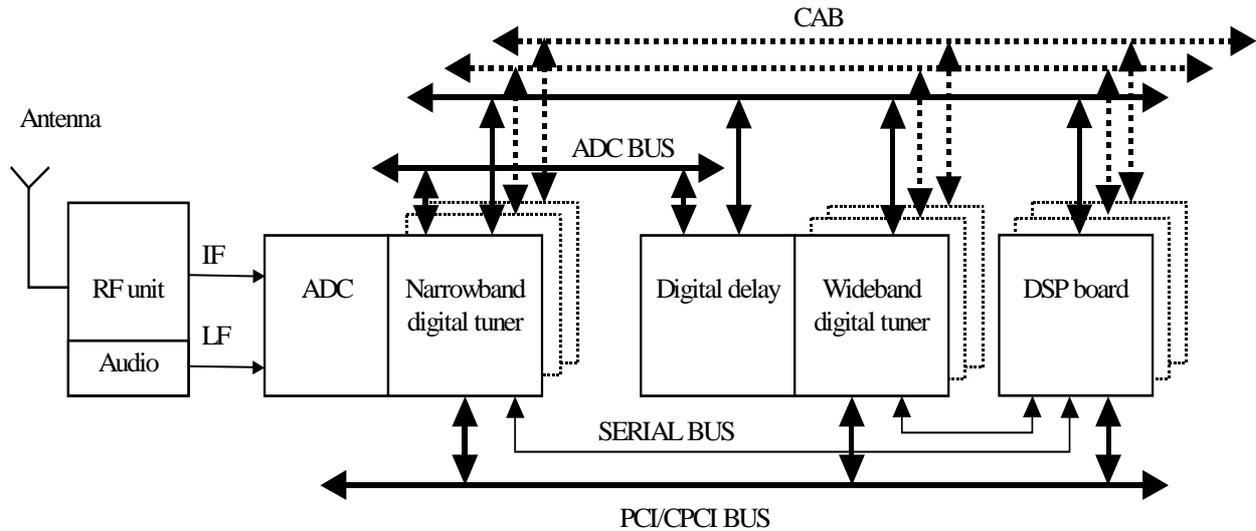
Fig. 1. Block diagram of MSR

MSR can also work as a combined search and reception receiver. In this case we assume that we don't know signal parameters, modulation type, frequency range etc. Typical configuration consists of NTB, WTB and DSP boards. The wideband receiver is used for signal detection. DSP procedures evaluate signal bandwidth, centre frequency etc. This parameters are then passed to the NTB and the narrowband tuner is tuned to the desired signal. Then DSP can analyse modulation type, signal parameters, data rate etc. and perform its demodulation. In this configuration NTB uses a delayed signal from the ADC bus, to compensate computational time of detection procedures. It enables the "follow up" detection of frequency hopping signals, CHIRP signals and BURST-s reception.

For multi-channel applications it is also possible to use multiple boards of given type. They work synchronously to avoid signal intermodulations.

4. Narrowband Tuner Board

The MSR can process either analog or digital signals (fig. 2). It can use two signals from the external receiver: high or intermediate frequency signals (IF, RF) and audio output (LF). The first one is used for analysis and demodulation of analog and digitally modulated signals. It can be also used for selection of particular channels from the FM signals with frequency divided multiplexing (FM-FDM) and the analysis of signals with secondary FM modulation. The IF signal can be either analog or digital IQ. The audio input can be used for analysis of low frequency demodulated signals, wired modems etc.

Analog signals are conditioned using low-pass filters with 30 MHz and 50 kHz bandwidth respectively, and adjustable amplifiers. The amplifiers are controlled by DAC and can be used for analog gain control. Analog to digital conversion is performed with accuracy of 12 bits and sampling frequency of 65 MSps. Digital signal from the ADC is transmitted to the ADC bus and the narrowband digital tuner (HSP 50214). The tuner contains tuneable quadrature digital local generator, complex mixer and programmable decimating filters [3]. The filters are FIR filters that provide ideally linear phase characteristics. Output signal can be phase-adjusted using poli-phase interpolator. Signal on the output of the down-converter is a complex signal with zero centre frequency and sampling frequency at least 1.7 times higher than the selected 3 dB bandwidth. The tuner also contains frequency discriminator that can be used for phase locked loop demodulation, or as a general purpose FM demodulator.

Optional second tuner is used for the FM signal analysis. In this case the first tuner works as a FM demodulator and its output signal is a source of data for the second tuner that extracts particular channels from the FM-FDM signal. Output signal can be transmitted by CAB to DSP for analysis and through the PCI to the PC for storage. Stored signals can also be played back from the HDD and transmitted to the DSP for multiple analysis. Serial buses are used by the DSP for remote control of tuners and the DAC.
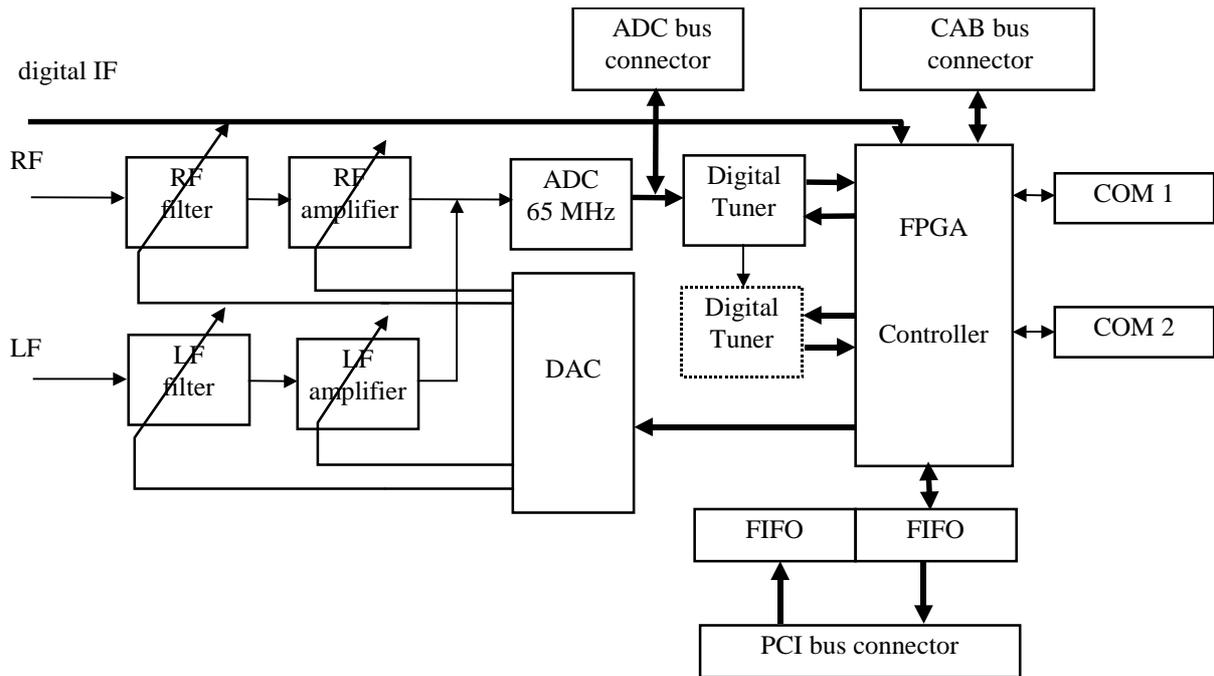
Fig. 2. Block diagram of the narrowband tuner board

5. Wideband Tuner Board

The WTB board consists of two functional blocks: the delay line and the tuner. Input signal is a 12-bit digital signal from the ADC bus (fig. 3). The input signal can be delayed using the "swing buffer". The buffer consists of at least 2 RAM blocks. These blocks are alternatively used for writing and reading operations. The shift between write and read pointers is always the same and is equal to the block size. The input data clock is fixed, so the block size determines also the maximum delay. To achieve the variable delay, the FPGA controller uses only a selected area from each memory block to store the data. The delayed signal can be processed by the wideband tuner or transmitted back to other boards (e.g. narrowband tuner) using upper half of the ADC bus. Maximum size of memory is 256Mx16 and it gives delay up to 2 seconds.

The wideband tuner (GC1012A) is a digital down-converter [4]. Signals are converted to the baseband, filtered using low-pass filters and decimated. The decimation factor value is programmed at rates 2...64. The decimator can also be skipped. The pass-band of the output filter covers about 80% of the output bandwidth. The output signal can be a complex or real one. The spectrum can be also inverted or shifted by a half of the output sampling rate. This solution is very flexible and enables the signal acquisition in a form, corresponding to currently performed functions.

The narrowband tuner (HSP 50214) is an optional circuit. It can work as the second tuner, after the signal is processed by the wideband tuner or they can work in parallel way. If the wideband tuner works as a front–end mixer and filter, its output signal can be configured as a real one. The signal spectrum is then shifted by a half of the output sampling rate. The signal can be fed to the input of the narrowband tuner, that performs further filtration and decimation. It can be used both for analysis of very narrowband signals, when the decimation factor of a single tuner is insufficient and for reception of signals in presence of strong adjacent interfering signals where high selectivity is required.

In the parallel configuration, the wideband tuner can be used for wideband signal reception, whereas the other one is used for frequency offset tracking, CHIRP signals carrier frequency detection or follow-up reception of FH signals. In this case the narrowband tuner can use a delayed input signal to compensate the calculation time in the DSP.

Output signals can be transmitted by the CAB to the DSP for further analysis. The PCI interface is used mainly for board configuration. The serial bus is used for remote control of tuners and the delay line by the DSP.

Fig. 3 block diagram

ADC bus connector	CAB bus connector	

```
                                              COM
              FPGA
                                        Wideband
   FIFO                                 Digital Tuner
            controller
                                        Narrowband
   DRAM                                 Digital Tuner
   DRAM
   DRAM            FIFO    FIFO
   DRAM
                 PCI bus connector
```
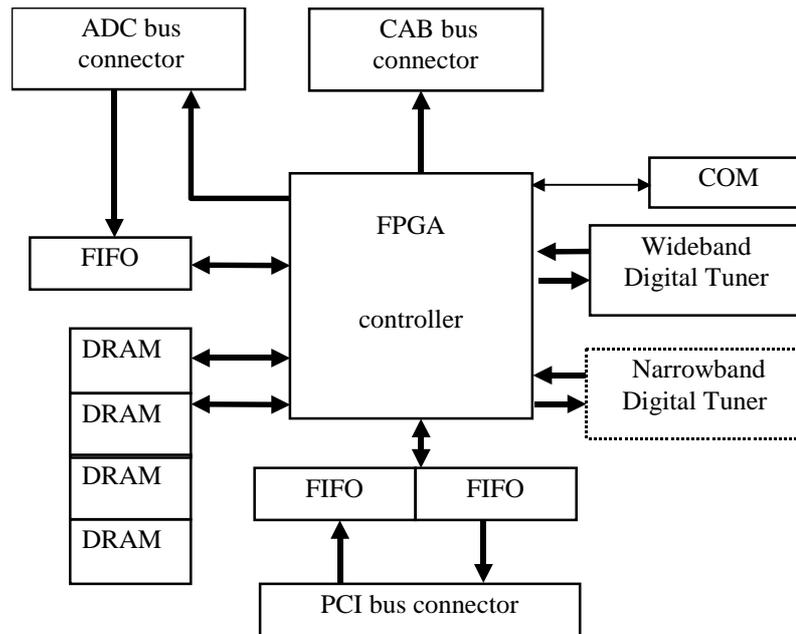
Fig. 3. Block diagram of the wide-band tuner board

6. Digital Signal Processors Board

The Python/C67 PCI/CPCI board is a multi-DSP processing card exploiting Texas Instrument's TMS320C6701 floating point DSP (fig. 5.) [5]. The Python/C67 supports up to four TMS320C6701 DSPs interconnected via high-speed communication links allowing data to be communicated quickly between processors. This high-speed architecture is ideal for implementing either pipelined or parallel image and signal processing applications. The Python/C67 is an expansion capable and connected to other boards through the 32-bit CAB (Coreco Auxiliary Bus) at 50 MHz. Key features of the board are:

- up to four TMS320C6701s at 167 MHz;
- four GFLOPs (peak) processing power on a single board;
- 512 KB of SBSRM/DSP;
- 16 MB of SDRAM/DSP;
- 4 MB of shared EDORAM;
- direct inter-DSP communication links;
- on-board interface to PMC module;
- 32-bit CAB bus interface at 50 MHz;
- integrated JTAG controller;
- on-board Intel i960 controller.

The board is very flexible and provides fast communications interfaces that make it very suitable for real time applications. CPCI version is software compatible with PCI version that enables easy upgrade to the ruggedized version of MSR.
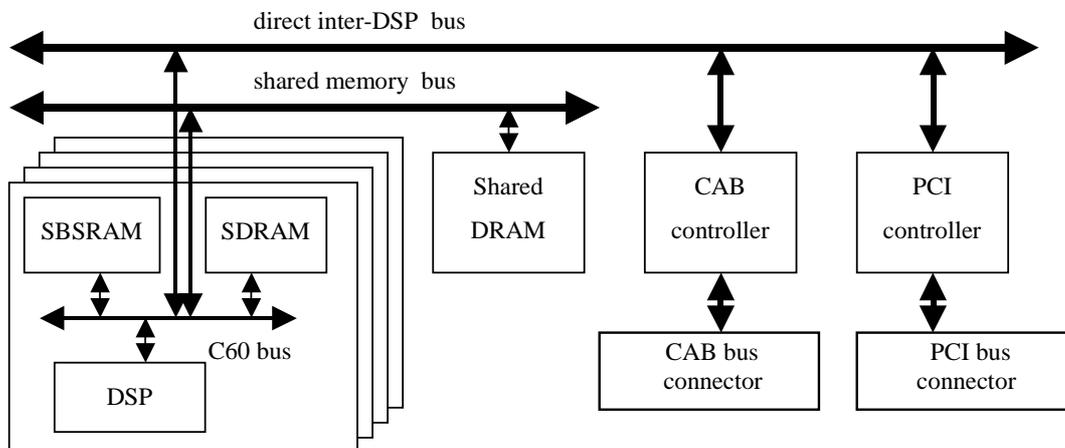
Fig. 4 block diagram

```
  direct inter-DSP  bus
     shared memory  bus

                          Shared      CAB        PCI
   SBSRAM   SDRAM         DRAM        controller  controller

              C60 bus                  CAB bus     PCI bus
      DSP                              connector   connector
```

Fig. 4. Block diagram of CORECO PYTHON C67 board.

3. Software structure

MSR software is a modular multilevel application. The lowest level is related to board configurations, data transfers, remote control, tasks management etc. and is invisible for the user. Higher level modules perform signal acquisition, analysis, detection, recognition, demodulation and decoding.

Signal analysis can be performed either manually or in automated manner. It is based on analysis of complex signals. Real and imagine parts, constellation, momentary magnitude, phase, and frequency time plots are available. To determine signal bandwidth and carrier frequency FFT, mean FFT, maximum FFT and waterfall calculations are performed. Precise parameters measurement is possible on the basis of variety of histograms.

Data rate can be determined either using histograms or eye patterns. Structure of transmitted data can be analysed on the basis of facsimile display, where each data bit is depicted as a horizontal line. For plain transmissions it is possible to determine the length of bytes, packets structures and protocols. It enables useful data extraction. Received bit flow can be decoded using user defined decoder. Applying selected descrambler it can reject synchronisation words, split bits into several channels and decode them according to specified transmission alphabet [6].

Signal recognition is performed by the DSP. Signal statistics are calculated, and using them as distinctive features, fuzzy logic test is evaluated for modulation scheme classification [7]. According to selected signal type, basic parameters as data rate, carrier frequency and frequency shift are calculated. All these parameters are used for demodulator selection and its proper configuration.

After the recognition process is completed successfully, all necessary parameters for signal demodulation are known. If not, the system operator is prompted to set them properly. The next step is signal demodulation performed by DSP-s in software way, using optimum or sub-optimum algorithms, that increase the resistance of such demodulators to different types of jamming. Adaptive algorithms can eliminate inter symbol interferences and perform radio channel modelling. Equalisation of channel parameters can eliminate multi-path propagation effects. In the MSR following demodulators are implemented:
- discriminator based FSK,
- correlation based FSK,
- M-ary discriminator based FSK,
- 2 PSK,
- 2,4,8 DPSK version A,
- 2,4 DPSK version B,
- 16 QAM.

The demodulated signal is decoded using several types of decoders. To select the proper one, autocorrelation and statistics analysis is performed first. It enables selection of proper descrambler, determination of packets' sizes, flags identification etc. For most transmissions a Viterbi decoder is used. According to the further statistic analysis a proper alphabet can be selected and if the transmission was plain MSR could display the received information.

8. Conclusions

The designed modular receiver is a flexible platform for multilevel analysis and reception of radio signals. Its performance and computational power can be adjusted according to current user needs. Modular software enables implementation of both wide-band and narrowband signals analysis. The solution is flexible and it can be used in advanced radio-monitoring systems, EW applications etc. The MSR can be also supplemented with digital up-conversion board to create a fully operating software radio.

References

1. Place J., Ker D., Schafer Rd., „*Joint Tactical Radio System*", Milcom 2000, pp.209-214.
2. Mitola J. III, *"SDR Architecture Refinement for JTRS",* Milcom 2000, Pp 214-219.
3. Intersil Corp. *"HSP 50016 datasheet",* June 1999.
4. Graychip Inc. *"GC1012A –digital tuner chip datasheet"*, February 1998.
5. Coreco Inc. *"PYTHON/C6 – datasheet"*, 1998.
6. Lopatka Jerzy: *Adaptive Multiwaveform Demodulator Of Radio Signals*", 5th International Symposium on Digital Signal Processing for Communication, Perth 1999, pp. 37-43.
7. Lopatka Jerzy, Pedzisz Maciej: *Automatic Modulation Classification Using Statistical Moments and a Fuzzy Classifier,* World Computer Congress, International Conference on Signal Processing, Beijing, 2000, vol. ICSP, pp. 121-127.